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A Buck & Boost based Grid Connected PV Inverter Maximizing Power Yield from Two PV Arrays in Mismatched Environmental Conditions

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***Abstract*—A single phase grid connected transformerless photo voltaic (PV) inverter which can operate either in buck or in boost mode, and can extract maximum power simultaneously from two serially connected subarrays while each of the subarray is facing different environmental conditions, is presented in this paper. As the inverter can operate in buck as well as in boost mode depending on the requirement, the constraint on the minimum number of serially connected solar PV modules that is required to form a subarray is greatly reduced. As a result power yield from each of the subarray increases when they are exposed to different environmental conditions. The topological configuration of the inverter and its control strategy are designed so that the high frequency components are not present in the common mode voltage thereby restricting the magnitude of the leakage current associated with the PV arrays within the specified limit. Further, high operating efficiency is achieved throughout its operating range. A detailed analysis of the system leading to the development of its mathematical model is carried out. The viability of the scheme is confirmed by performing detailed simulation studies. A 1.5 kW laboratory prototype is developed, and detailed experimental studies are carried out to corroborate the validity of the scheme.**

***Index Terms*—Grid connection, Single phase, Transformerless, Buck & Boost based PV inverter, Maximum power point, Mismatched environmental condition, Series connected module.**

I. Introduction

THE major concern of a photo voltaic (PV) system is to ensure optimum performance of individual PV modules in a PV array while the modules are exposed to different environmental conditions arising due to difference in insolation level and/or difference in operating temperature. The presence of mismatch in operating condition of modules significantly reduces the power output from the PV array [1]. The problem with the mismatched environmental conditions (MEC) becomes significant if the number of modules connected in series in a PV array is large. In order to achieve desired magnitude for the input dc link voltage of the inverter of a grid connected transformerless PV system, the requirement of series connected modules becomes high. Therefore, the power output from a grid connected transformerless (GCT) PV system such as single phase GCT (SPGCT) inverter based systems derived from H-bridge [2], [3] and neutral point clamp (NPC) inverter based systems [4], [5] get affected significantly during MEC.

In order to address the problem arising out of MEC in a PV system, various solutions are reported in the literature. An exhaustive investigation of such techniques has been presented in [6]. Power extraction during MEC can be increased by choosing proper interconnection between PV modules [6], [7] or by tracking global maximum power point (MPP) of PV array by employing complex MPP tracking (MPPT) algorithm [6], [8]. However, these techniques are not effective for low power SPGCT PV system. Similarly, reconfiguration of the PV modules in a PV array by changing the electrical connection of PV modules [9], [10] is not effective for SPGCT PV system due to the considerable increment in component count and escalation in operating complexity. In order to extract maximum power from each PV module during MEC, attempts have been made to control each PV module in a PV array either by having a power electronic equalizer [11] or by interfacing a dc to dc converter [1], [12]- [14]. Schemes utilizing power electronic equalizer require large component count thereby increasing the cost and operation complexity of the system. The scheme presented in [1] uses generation control circuit (GCC) to operate each PV module at their respective MPP wherein the difference in power between each module is only processed through the GCC. Scheme presented in [12] uses shunt current compensation of each module as well as series voltage compensation of each PV string in a PV array to enhance power yield during MEC. The schemes based on module integrated converter [13], [14] use dedicated dc to dc converter integrated with each PV module. However, the efficiency of the aforesaid schemes are low due to the involvement of large number of converter stages, and further in these schemes the component count is high and hence they face similar limitations as that of power electronic equalizer based scheme. Instead of ensuring MPP operation of each and every module, certain number of modules are connected in series to form a string and the so formed strings are then made to operate under MPP in [15], [16]. Even then there is not much reduction in overall component count and control complexity [6].

In order to simplify the control configuration and to reduce the component count, schemes reported in [17], [18] combine all the PV modules into two subarrays, and then each of the subarray is made to operate at their respective MPP. However,

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the reported overall efficiency of both the schemes are poor. By introducing a buck and boost stage in SPGCT PV inverter, power extraction during MEC is improved in [19]- [21]. Further, as a consequence of the presence of the intermediate boost stage, the requirement of series connected PV modules in a PV array has become less. In the schemes presented in [19]- [21], the switches of either the dc to dc converter stage or inverter stage operate at high frequency, as a result there is a considerable reduction in the size of the passive element count, thereby improving the operating efficiency of these schemes. Further, the reported efficiency of [20] and [21] is 1-2 % higher than that of [19].

An effort has been made in this paper to divide the PV modules into two serially connected subarrays and controlling each of the subarray by means of a buck and boost based inverter so that optimum power evacuation from the subarrays is ascertained during MEC. This process of segregation of input PV array into two subarrays reduces the number of series connected modules in a subarray almost by half compared to that of the schemes proposed in [20], [21]. The topological structure and control strategy of the proposed inverter ensure that the magnitude of leakage current associated with the PV arrays remains within the permissible limit. Further, the voltage stress across the active devices is reduced almost by half compared to that of the schemes presented in [20], [21], hence very high frequency operation without increasing the switching loss is ensured. High frequency operation also leads to the reduction in the size of the passive elements. As a result the operating efficiency of the proposed scheme is high. The measured peak efficiency and the European efficiency (η_{euro}) of the proposed scheme is found to be 97.65% and 97.02% respectively.

The detailed operation of the proposed inverter with mathematical validation is explained in Section II. Afterwards the mathematical model of the proposed inverter has been derived in Section III followed by the philosophy of control strategy in Section IV. The criteria to select the values of the output filter components are presented in Section V. The proposed scheme is verified by performing extensive simulation studies and the simulated performance is presented in Section VI. A 1.5 kW laboratory prototype of the proposed inverter has been fabricated to carry out thorough experimental studies. The measured performances of the scheme which confirm its viability are presented in Section VII.

II. Proposed Inverter and its Operation

The schematic of the proposed Dual Buck & Boost based Inverter (DBBI) which is depicted in Fig. 1 is comprising of a dc to dc converter stage followed by an inverting stage. The dc to dc converter stage has two dc to dc converter segments, $CONV_1$ and $CONV_2$ to service the two subarrays, PV_1 and PV_2 of the solar PV array. The segment, $CONV_1$ is consisting of the self-commutated switches, S_1 along with its anti-parallel body diode, D_1, S_3 along with its anti-parallel body diode, D_3, the free wheeling diodes, D_{f1}, D_{f3} and the filter inductors and capacitors, L_1, C_{f1}, and C_{o1}. Similarly, the segment, $CONV_2$ is consisting of the self-commutated switches, S_2 along with its anti-parallel body diode, D_2, S_4 along with its anti-parallel body diode, D_4, the free wheeling diodes, D_{f2}, D_{f4} and the filter inductors and capacitors, L_2, C_{f2}, and C_{o2}. The inverting stage is consisting of the self-commutated switches, S_5, S_6, S_7, S_8, and their corresponding body diodes, D_5, D_6,D_7 and D_8 respectively. The inverter stage is interfaced with the grid through the filter inductor, L_g. The PV array to the ground parasitic capacitance is modeled by the two capacitors, C_{pv1} and C_{pv2}.

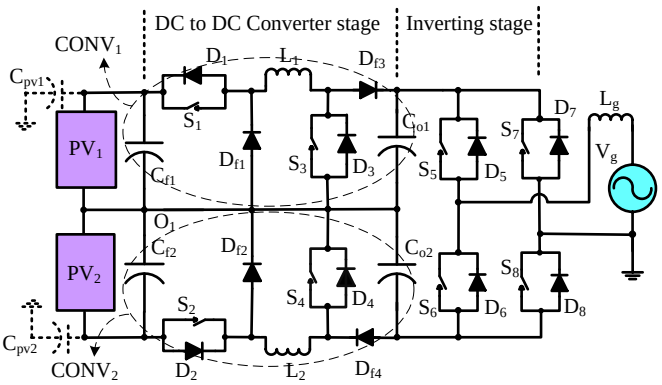

Fig. 1. Dual Buck & Boost based Inverter (DBBI)

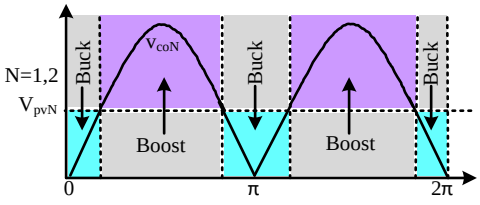

Fig. 2. Buck stage and Boost stage of the proposed inverter

Considering Fig. 2, $CONV_1$ operates in buck mode when $V_{pv1} \geq v_{co1}$, while $CONV_2$ operates in buck mode when $V_{pv2} \geq v_{co2}$. V_{pv1}, V_{pv2} are the MPP voltages of PV_1 and PV_2 and v_{co1}, v_{co2} are the output voltages of $CONV_1$ and $CONV_2$ respectively. During buck mode duty ratios of the switches, S_1 and S_2 are varied sinusoidally to ensure sinusoidal grid current (i_g) while S_3 and S_4 are kept off. When $V_{pv1} < v_{co1}$, $CONV_1$ operates in boost mode while $CONV_2$ operates in boost mode when $V_{pv2} < v_{co2}$. During boost mode duty ratios of the switches, S_3 and S_4 are varied sinusoidally to ensure sinusoidal i_g while S_1 and S_2 are kept on throughout this mode. The sinusoidal switching pulses of the switches of $CONV_1$ and $CONV_2$ are synchronized with the grid voltage, v_g to accomplish unity power factor operation. The switches, S_5 and S_8 are kept on and switches S_6 and S_7 are kept off permanently during the entire positive half cycle (PHC) while during entire negative half cycle (NHC), the switches, S_6 and S_7 are kept on and switches, S_5 and S_8 are kept off permanently. All the operating states of the proposed inverter are depicted in Fig. 3.

When the insolation level and ambient temperature of subarray PV_1 are different from that of PV_2, the MPP parameters

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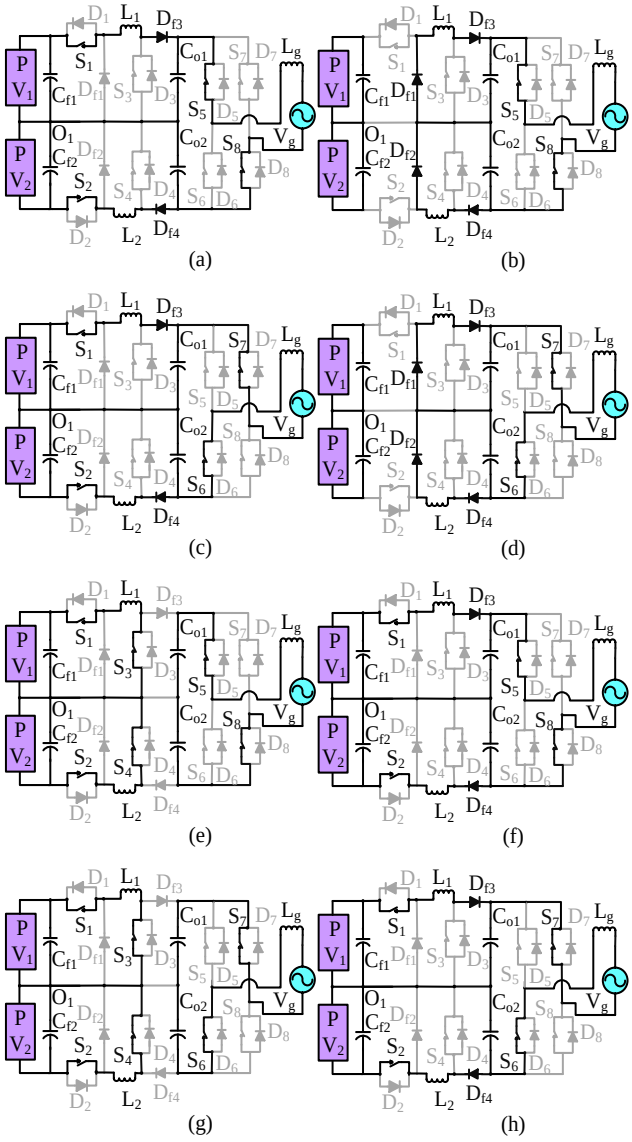

Fig. 3. Operating states of DBBI: (a) Active and (b) Freewheeling states in buck mode of PHC, (c) Active and (d) Freewheeling states in buck mode of NHC, (e) Active and (f) Freewheeling states in boost mode of PHC, (g) Active and (h) Freewheeling states in boost mode of NHC

of the two subarrays, V_{pv1} and V_{pv2}, MPP current, I_{pv1} and I_{pv2} correspond to PV_1 and PV_2 respectively and power at MPP, P_{pv1} and P_{pv2} correspond to PV_1 and PV_2 respectively differ from each other. By considering that both the subarrays are operating at their respective MPP and neglecting the losses incurred in power processing stages, the average power involved with C_{o1} and C_{o2}, P_{co1} and P_{co2} over a half cycle can be assumed equal to the power extracted from PV_1 and PV_2. Therefore,

$$P_{co1} = P_{pv1} \quad \& \quad P_{co2} = P_{pv2} \tag{1}$$

The power injected to the grid averaged over a half cycle, P_g can be written as

$$P_g = P_{pv1} + P_{pv2} \tag{2}$$

Further, at any half cycle

$$v_g = v_{co1} + v_{co2} \tag{3}$$

Hence, the instantaneous injected power to the grid, p_g can be written as

$$p_g = v_g i_g = (v_{co1} + v_{co2}) i_g \tag{4}$$

wherein v_{co1} and v_{co2} denote the instantaneous quantities of V_{co1} and V_{co2} respectively. As i_g is in-phase with v_g,

$$I_g = \frac{P_g}{V_g} \tag{5}$$

wherein V_g and I_g denote rms values of v_g and i_g respectively. The power injected to the grid can be expressed as

$$\begin{aligned} P_g &= \frac{1}{\pi}\int_0^{\pi} p_g \, d(\omega t) \\ &= \frac{1}{\pi}\int_0^{\pi} v_{co1} i_g \, d(\omega t) + \frac{1}{\pi}\int_0^{\pi} v_{co2} i_g \, d(\omega t) \quad (6) \\ &= P_{co1} + P_{co2} \quad (7) \end{aligned}$$

As v_{co1} and v_{co2} are synchronized with v_g. Hence

$$\begin{aligned} P_{co1} &= \frac{1}{\pi}\int_0^{\pi} V_{co1m} \sin(\omega t) \, I_{gm} \sin(\omega t) \, d(\omega t) \\ &= \frac{V_{co1m} I_{gm}}{2} \end{aligned} \tag{8}$$

Similarly,

$$P_{co2} = \frac{V_{co2m} I_{gm}}{2} \tag{9}$$

wherein the amplitudes of v_{co1}, v_{co2} and i_g are denoted as V_{co1m}, V_{co2m} and I_{gm} respectively. Combining (1), (8) and (9)

$$V_{co1m} = \frac{2P_{pv1}}{I_{gm}} = \frac{\sqrt{2}P_{pv1}}{I_g} = \frac{\sqrt{2}P_{pv1}}{P_g/V_g} \tag{10}$$

$$V_{co2m} = \frac{2P_{pv2}}{I_{gm}} = \frac{\sqrt{2}P_{pv2}}{I_g} = \frac{\sqrt{2}P_{pv2}}{P_g/V_g} \tag{11}$$

Similarly by combining (2), (10) and (11),

$$V_{co1m} = \frac{V_m P_{pv1}}{P_{pv1} + P_{pv2}} \quad \& \quad V_{co2m} = \frac{V_m P_{pv2}}{P_{pv1} + P_{pv2}} \tag{12}$$

The voltage templates of v_{co1} and v_{co2} appear as full wave rectified sinusoidal waveform with amplitudes, V_{co1m} and V_{co2m} respectively. V_m is the amplitude of v_g. It can be deduced from (12) that the magnitudes of V_{co1m} and V_{co2m} are decided by the power extracted from each of the subarray. If the power extracted from PV_1 is less than PV_2, then $V_{co1m} < V_{co2m}$, whereas $V_{co2m} < V_{co1m}$ if power extracted from PV_2 is less than PV_1. During buck mode, the duty ratios, d_1 of S_1 and d_2 of S_2 vary sinusoidally with an amplitude d_{1m} and d_{2m}, wherein

$$d_{1m} = \frac{V_{co1m}}{V_{pv1}} \quad \& \quad d_{2m} = \frac{V_{co2m}}{V_{pv2}} \tag{13}$$

while during boost mode the duty ratios, d_3 of S_3 and d_4 of S_4 vary sinusoidally with amplitude d_{3m} and d_{4m}, wherein

$$d_{3m} = 1 - \frac{V_{pv1}}{V_{co1m}} \quad \& \quad d_{4m} = 1 - \frac{V_{pv2}}{V_{co2m}} \tag{14}$$

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The $CONV_1$ and $CONV_2$ are having the same output current i_g. Hence, the input side currents before getting filtered by input filter capacitors of $CONV_1$, i_{sw1} and $CONV_2$, i_{sw2} can be related with i_g in the buck mode by considering the switching cycle average of corresponding quantities as follows

$$\langle i_{sw1}\rangle_{T_s} = \langle d_1\rangle_{T_s}\langle i_g\rangle_{T_s} \tag{15}$$

$$\langle i_{sw2}\rangle_{T_s} = \langle d_2\rangle_{T_s}\langle i_g\rangle_{T_s} \tag{16}$$

Similarly by considering switching cycle average of corresponding quantities the relation between i_{sw1}, i_{sw2} and i_g can be deduced during boost mode as

$$\langle i_{sw1}\rangle_{T_s} = \langle \frac{1}{1-d_3}\rangle_{T_s}\langle i_g\rangle_{T_s} \tag{17}$$

$$\langle i_{sw2}\rangle_{T_s} = \langle \frac{1}{1-d_4}\rangle_{T_s}\langle i_g\rangle_{T_s} \tag{18}$$

Therefore, it can be inferred from (12) and (13) that if the insolation level of PV_1 is lower than that of PV_2, during buck mode, $d_{1m} < d_{2m}$, thereby $\langle d_1\rangle_{T_s} < \langle d_2\rangle_{T_s}$ whereas during boost mode as per (12) and (14), $d_{3m} < d_{4m}$, thereby $\langle d_3\rangle_{T_s} < \langle d_4\rangle_{T_s}$. Hence, it can be concluded from (15), (16), (17) and (18) that in any operating mode, $\langle i_{sw1}\rangle_{T_s} < \langle i_{sw2}\rangle_{T_s}$, therefore $I_{pv1} < I_{pv2}$. Following the same argument, $I_{pv1} > I_{pv2}$ if the insolation level of PV_1 is higher than that of PV_2.

Considering Fig. 1 it can be noted that during operation in PHC, $v_{cpv1} = v_{co2} + V_{pv1}$, $v_{cpv2} = v_{co2} - V_{pv2}$ while during NHC $v_{cpv1} = -v_{co1} + V_{pv1}$, $v_{cpv2} = -v_{co1} - V_{pv2}$, wherein v_{cpv1} and v_{cpv2} are the voltages impressed across C_{pv1} and C_{pv2} respectively. Hence, the voltages across C_{pv1} and C_{pv2} contain significant amount of dc and low frequency components which also ensures that the magnitude of the leakage current is maintained within the limit specified in the standard, VDE 0126-1-1, and also cited in [23].

III. Mathematical Model of the Proposed Scheme

A small signal modeling of the proposed inverter has been carried out for buck mode and boost mode of operation. Fig. 4(a) and (b) represent the equivalent circuit of the proposed inverter while it operates in buck mode whereas Fig. 4(c) and (d) represent the equivalent circuit of the converter while it operates in boost mode. R_{L1}, R_{L2}, R_g, R_{co1} and R_{co2} are the parasitic resistances of L_1, L_2, L_g, C_{o1} and C_{o2} respectively. As indirect grid current control method [21] is adopted to control i_g, the quantities i_{L1}, i_{L2}, v_{co1}, v_{co2} and i_g are considered to be the state variables. The state equations representing the buck mode of operation of the inverter are derived to be (19), (20) by considering the equivalent circuits of Fig. 4(a), (b) while the state equations for boost mode are derived to be (21), (19) by considering the equivalent circuits of Fig. 4(c), (d).

$$\begin{bmatrix} \dot{i}_{L1}(t) \\ \dot{i}_{L2}(t) \\ \dot{v}_{co1}(t) \\ \dot{v}_{co2}(t) \\ \dot{i}_g(t) \end{bmatrix} = \begin{bmatrix} -\frac{R_{L1}+R_{co1}}{L_1} & 0 & -\frac{1}{L_1} & 0 & \frac{R_{co1}}{L_1} \\ 0 & -\frac{R_{L2}+R_{co2}}{L_2} & 0 & -\frac{1}{L_2} & \frac{R_{co2}}{L_2} \\ \frac{1}{C_{o1}} & 0 & 0 & 0 & -\frac{1}{C_{o1}} \\ 0 & \frac{1}{C_{o2}} & 0 & 0 & -\frac{1}{C_{o2}} \\ \frac{R_{co1}}{L_g} & \frac{R_{co2}}{L_g} & \frac{1}{L_g} & \frac{1}{L_g} & -\frac{R_{co1}+R_{co2}+R_g}{L_g} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{co1}(t) \\ v_{co2}(t) \\ i_g(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} & 0 & 0 \\ 0 & \frac{1}{L_2} & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{L_g} \end{bmatrix} \begin{bmatrix} v_{pv1}(t) \\ v_{pv2}(t) \\ v_g(t) \end{bmatrix} \tag{19}$$

$$\begin{bmatrix} \dot{i}_{L1}(t) \\ \dot{i}_{L2}(t) \\ \dot{v}_{co1}(t) \\ \dot{v}_{co2}(t) \\ \dot{i}_g(t) \end{bmatrix} = \begin{bmatrix} -\frac{R_{L1}+R_{co1}}{L_1} & 0 & -\frac{1}{L_1} & 0 & \frac{R_{co1}}{L_1} \\ 0 & -\frac{R_{L2}+R_{co2}}{L_2} & 0 & -\frac{1}{L_2} & \frac{R_{co2}}{L_2} \\ \frac{1}{C_{o1}} & 0 & 0 & 0 & -\frac{1}{C_{o1}} \\ 0 & \frac{1}{C_{o2}} & 0 & 0 & -\frac{1}{C_{o2}} \\ \frac{R_{co1}}{L_g} & \frac{R_{co2}}{L_g} & \frac{1}{L_g} & \frac{1}{L_g} & -\frac{R_{co1}+R_{co2}+R_g}{L_g} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{co1}(t) \\ v_{co2}(t) \\ i_g(t) \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{L_g} \end{bmatrix} \begin{bmatrix} v_{pv1}(t) \\ v_{pv2}(t) \\ v_g(t) \end{bmatrix} \tag{20}$$

$$\begin{bmatrix} \dot{i}_{L1}(t) \\ \dot{i}_{L2}(t) \\ \dot{v}_{co1}(t) \\ \dot{v}_{co2}(t) \\ \dot{i}_g(t) \end{bmatrix} = \begin{bmatrix} -\frac{R_{L1}}{L_1} & 0 & 0 & 0 & 0 \\ 0 & -\frac{R_{L2}}{L_2} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{C_{o1}} \\ 0 & 0 & 0 & 0 & -\frac{1}{C_{o2}} \\ 0 & 0 & \frac{1}{L_g} & \frac{1}{L_g} & -\frac{R_{co1}+R_{co2}+R_g}{L_g} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{co1}(t) \\ v_{co2}(t) \\ i_g(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} & 0 & 0 \\ 0 & \frac{1}{L_2} & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{L_g} \end{bmatrix} \begin{bmatrix} v_{pv1}(t) \\ v_{pv2}(t) \\ v_g(t) \end{bmatrix} \tag{21}$$

The state space averaging based technique is adopted as the grid frequency, f_g is adequately lower than the switching frequency, f_s. In order to simplify the analysis, V_{pv1}, V_{pv2} and v_g are considered as stiff voltage sources, and the effect of input filter capacitors is neglected. The values of the system parameters are considered to be as follows: $R_{L1} = R_{L2} = 0.12\ \Omega$, $R_g = 0.04\ \Omega$, $R_{co1} = R_{co2} = 0.26\ \Omega$, $V_{pv1} = V_{pv2} = 130\ V$. Considering symmetry in operation of $CONV_1$ and $CONV_2$, and by applying state space averaging technique to (19), (20) and (21), the simplified transfer functions of $i_g(s)/d(s)$, $i_{L1}(s)/d(s)$ and $v_{co1}(s)/d(s)$ in s-domain during buck mode

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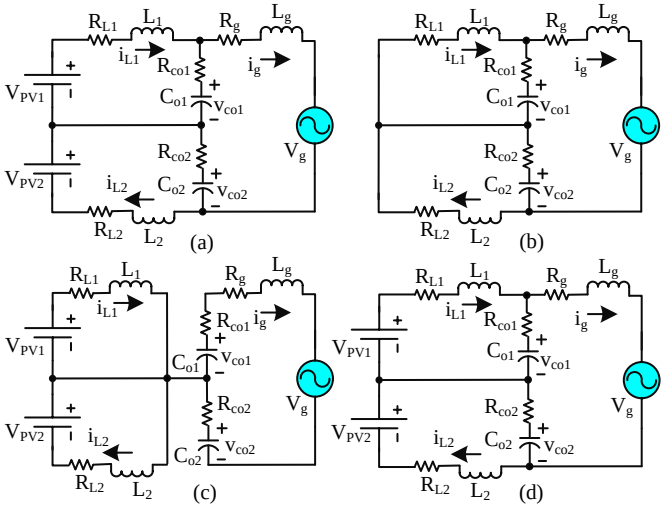

Fig. 4. Equivalent circuit in Buck mode (a) S_1, S_2 are ON (b) S_1, S_2 are OFF, in Boost mode (c) S_3, S_4 are ON (d) S_3, S_4 are OFF

are obtained as

$$\frac{i_g(s)}{d(s)} = \frac{2.87 \times 10^8 s + 2.2 \times 10^{14}}{s^3 + 2267 \times s^2 + 1.33 \times 10^9 s + 3 \times 10^{11}} \quad (22)$$

$$\frac{i_{L1}(s)}{d(s)} = \frac{2.17 \times 10^5 s^2 + 3.52 \times 10^8 s + 2.2 \times 10^{14}}{s^3 + 2267 \times s^2 + 1.33 \times 10^9 s + 3 \times 10^{11}} \quad (23)$$

$$\frac{v_{co1}(s)}{d(s)} = \frac{4.33 \times 10^{10} s + 1.3 \times 10^{13}}{s^3 + 2267 \times s^2 + 1.33 \times 10^9 s + 3 \times 10^{11}} \quad (24)$$

wherein, d is the duty ratio of component converters. Similarly, the simplified transfer functions of $i_g(s)/d(s)$, $i_{L1}(s)/d(s)$ and $v_{co1}(s)/d(s)$ in s-domain during boost mode are obtained as

$$\frac{i_g(s)}{d(s)} = \frac{-9487 s^2 - 9.7 \times 10^9 s + 2.1 \times 10^{14}}{s^3 + 2018 \times s^2 + 1.26 \times 10^9 s + 2.7 \times 10^{11}} \quad (25)$$

$$\frac{i_{L1}(s)}{d(s)} = \frac{2.4 \times 10^5 s^2 + 3.3 \times 10^9 s + 2.4 \times 10^{14}}{s^3 + 2018 \times s^2 + 1.26 \times 10^9 s + 2.7 \times 10^{11}} \quad (26)$$

$$\frac{v_{co1}(s)}{d(s)} = \frac{-2 \times 10^6 s^2 + 4.1 \times 10^{10} s + 4 \times 10^{12}}{s^3 + 2018 \times s^2 + 1.26 \times 10^9 s + 2.7 \times 10^{11}} \quad (27)$$

Due to the existence of symmetry, transfer functions for $i_{L2}(s)/d(s)$ and $v_{co2}(s)/d(s)$ remain the same as that of (23), (24) in buck mode and (26), (27) in boost mode respectively. Based on the derived transfer functions of the system, compensators are designed to achieve the phase margin of 90° for both the plants, and at the same time to maintain the desired total harmonic distortion (THD) for the grid current.

IV. Control Strategy of the Proposed Scheme

The control strategy of the proposed scheme is depicted in Fig. 5. The controller is designed to fulfill the following objectives: i) both subarrays operate at their corresponding MPP simultaneously, ii) sensing of output voltages, v_{co1} and v_{co2} are not required, iii) i_g is sinusoidal and is in-phase with v_g throughout the operating range. Two separate MPP trackers and two proportional integral (PI) controllers are employed to determine the value of P_{pv1} and P_{pv2} which are required

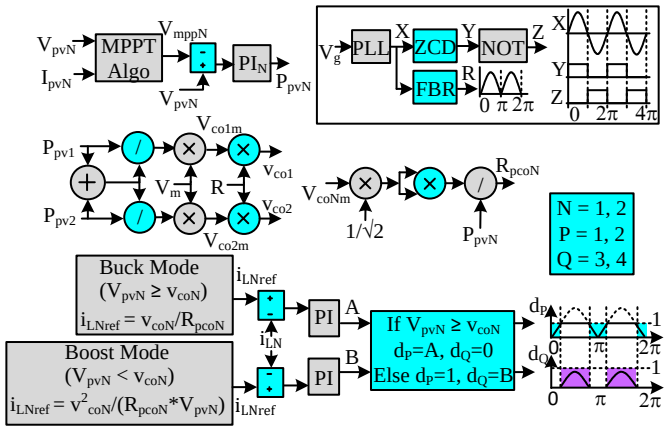

Fig. 5. Control configuration of the proposed inverter

to estimate V_{co1m} and V_{co2m}. Using (12), V_{co1m} and V_{co2m} are determined where the information of V_m is obtained from the phase locked loop (PLL). A rectified version of a unity sinusoidal function, R is generated from a unity sinusoidal function, X, synchronized with v_g, and is obtained from the same PLL. R is multiplied with V_{co1m} and V_{co2m} to estimate v_{co1} and v_{co2}. Hence, two voltage sensors which otherwise would have been required to determine v_{co1} and v_{co2} get eliminated. V_{pv1} and v_{co1} are compared to decide about the mode of operation (buck mode or boost mode) of $CONV_1$, while V_{pv2} and v_{co2} are compared to determine the mode of operation of $CONV_2$. RMS values of v_{co1} and v_{co2} are estimated which are then subsequently squared and are then divided by P_{pv1} and P_{pv2} to obtain the emulated effective resistances, R_{pco1} and R_{pco2} of the two component converters. Subsequently the reference current, i_{L1ref} of L_1 and the reference current, i_{L2ref} of L_2, are synthesized by utilizing (28) in the buck mode [21],

$$i_{L1ref} = \frac{v_{co1}}{R_{pco1}} \quad \text{and} \quad i_{L2ref} = \frac{v_{co2}}{R_{pco2}} \quad (28)$$

while for boost mode (29) is used to generate i_{L1ref} and i_{L2ref} [21].

$$i_{L1ref} = \frac{v_{co1}^2}{R_{pco1} V_{pv1}} \quad \text{and} \quad i_{L2ref} = \frac{v_{co2}^2}{R_{pco2} V_{pv2}} \quad (29)$$

The sensed inductor currents, i_{L1} and i_{L2} are compared with their corresponding references i_{L1ref} and i_{L2ref}. The errors so obtained are processed through two separate PI controllers to generate the required sinusoidal duty ratios for the switches, S_1 and S_2 during buck mode. Similarly, two separate PI controllers are engaged to process the generated errors to synthesize required sinusoidal duty ratios for switches S_3 and S_4 during boost mode. Signal Y is used to generate gating signals for S_5, S_8 while signal Z is used to generate gating signals for S_6, S_7 of the grid frequency unfolding inverter.

V. Selection of L_1, L_2, L_g & C_{o1}, C_{o2}

In order to select the value of the filter elements, L_1, L_2, L_g & C_{o1}, C_{o2} the design principle given in [24] is followed

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TABLE I
EMPLOYED PARAMETERS/ELEMENTS FOR SIMULATION AND EXPERIMENTAL PURPOSE

Parameter/elements	Value
V_g and f_g	220 V and 50 Hz
L_1, L_2, L_g & C_{o1}, C_{o2}	0.6 mH, 0.6 mH, 0.4 mH & 5 μF, 5 μF
C_{pv1} and C_{pv2}	0.1 μF
MPPT Algorithm	Incremental Conductance
Mosfets (S_1-S_8)	IPW60R041C6
Diodes (D_{f1}-D_{f4})	MBR40250
f_s of S_1-S_4 & f_s of S_5-S_8	50 kHz & 50 Hz
Digital Signal Controller	TMS320F28335

TABLE II
ESTIMATED VARIATIONS OF DIFFERENT QUANTITIES DURING APPLIED VARIATIONS ON INSOLATION AND TEMPERATURE OF TWO SUBARRAYS

Time in Second	0-1	1-2	2-3	3-4	4-5	5-6	6-7	7-8
Insol. in PV_1 (kW/m^2)	0.5	0.6	0.7	0.8	0.9	1.0	1.0	1.0
Insol. in PV_2 (kW/m^2)	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8
Temp. in PV_1 (^oC)	25	25	25	25	25	25	30	35
Temp. in PV_2 (^oC)	25	25	25	25	25	25	25	25
P_{pv1} (W)	331	397	463	529	595	661	638	621
P_{pv2} (W)	529	529	529	529	529	529	529	529
I_{gm} (A)	5.5	6.0	6.4	6.8	7.2	7.7	7.5	7.4
V_{co1m} (V)	120	133	147	155	165	173	170	168
V_{co2m} (V)	191	178	164	156	146	138	141	143
I_{L1m} (A)	5.7	7	8.1	9	10.3	11.4	11	10.7
I_{L2m} (A)	9	9	9	9	9	9	9	9

and the buck mode of operation for the inverter is considered. Values of L_1 and L_2 are obtained from the expression given in [24]

$$L_1 = \frac{V_{pv1}}{4\Delta I_{L1} f_s} \quad \& \quad L_2 = \frac{V_{pv2}}{4\Delta I_{L2} f_s} \tag{30}$$

wherein, V_{pv1} = V_{pv2} = 200 V, percentage peak to peak ripple of i_{L1} and i_{L2}, ΔI_{L1} and ΔI_{L2} are considered as 15% of rated peak current.

The values of C_{o1} and C_{o2} are obtained from the expression given in [24]

$$C_{o1} = \frac{xP_{co1}}{2\pi f_g V_{co1}^2} \quad \& \quad C_{o2} = \frac{xP_{co2}}{2\pi f_g V_{co2}^2} \tag{31}$$

wherein, V_{co1} = V_{co2} = 110 V, P_{co1} = P_{co2} = 750 W and factor x = 2.5%.

In order to achieve wide stability margin and large control bandwidth a value which is less than L_1 or L_2 is selected for L_g [24].

VI. SIMULATION STUDY

To demonstrate the efficacy of the proposed inverter a PV array consisting of two PV subarrays while each of the subarray having four series connected Canadian solar polycrystalline modules 'CS6P-165PE' [25] is considered. The MPP parameters of each subarray at standard test condition (STC) are as follows: V_{pv1} = V_{pv2} = 116 V, I_{pv1} = I_{pv2} = 5.7 A and P_{pv1} = P_{pv2} = 661 W. The parameters which are used to simulate the proposed inverter are indicated in Table I. Matlab-Simulink platform is utilized to simulate the performance of the proposed inverter.

The variation in insolation level and temperature with respect to time which is considered for the two subarrays to demonstrate the effectiveness of the proposed inverter are tabulated in Table II. Estimated variation of P_{pv1}, P_{pv2} along with the other parameters I_{gm}, V_{co1m}, V_{co2m}, peak of i_{L1} (I_{L1m}) and peak of i_{L2} (I_{L2m}) are also indicated in the same table. Fig. 6(a)-(c) represents the variation of P_{pv1}, P_{pv2}, V_{pv1}, V_{pv2}, I_{pv1}, I_{pv2} of the two subarrays and also demonstrate the ability of the proposed inverter to operate the two subarrays simultaneously at their respective MPP. Variation in i_g, i_{L1}, i_{L2}, v_{co1} and v_{co2} along with their magnified versions for two different insolation levels are depicted in Figs. 7 to 9. The estimated values of the aforementioned quantities as tabulated in Table II conform to that of obtained through simulation studies thereby ensuring the viability of the proposed scheme.

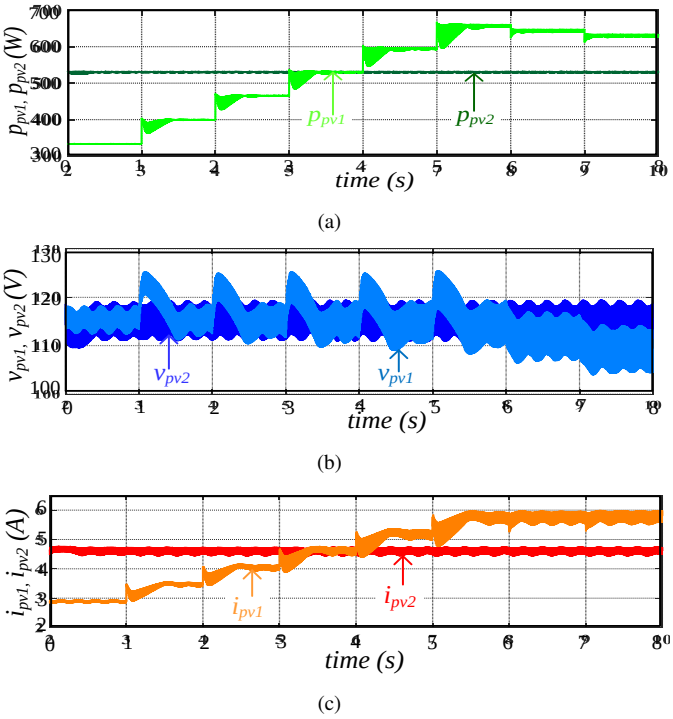

Fig. 6. Simulated waveform: Variation in (a) p_{pv1} and p_{pv2}, (b) v_{pv1} and v_{pv2}, (c) i_{pv1} and i_{pv2} during entire range of operation

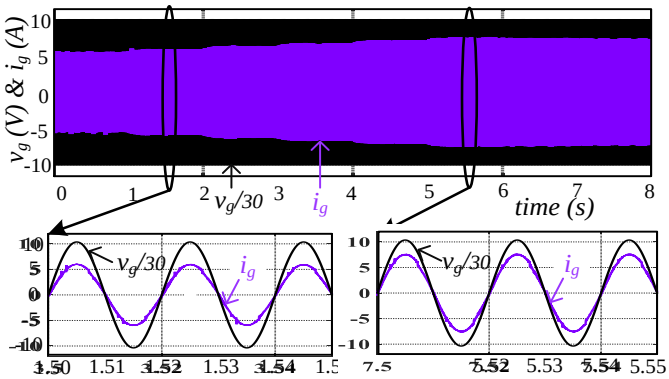

Fig. 7. Simulated waveform: v_g and i_g and their magnified views

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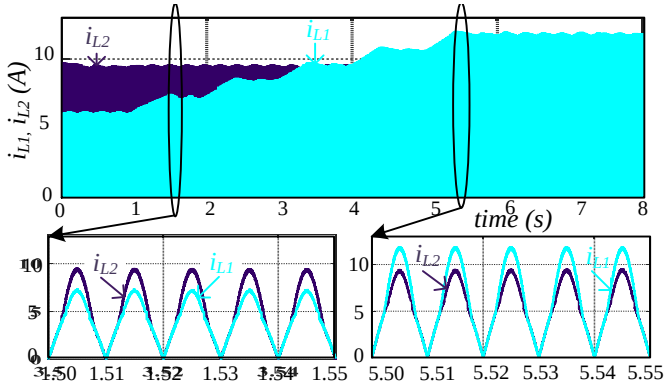

Fig. 8. Simulated waveform: i_{L1} and i_{L2} and their magnified views

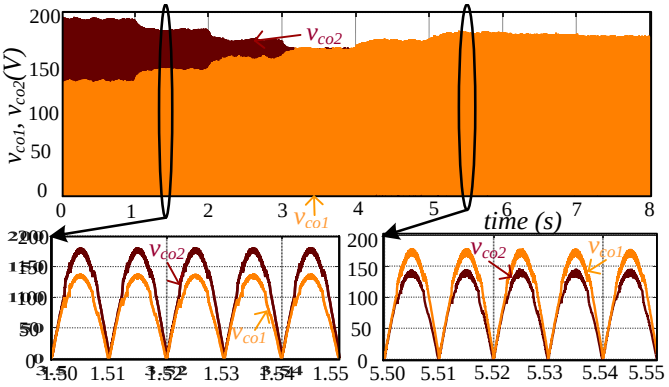

Fig. 9. Simulated waveform: v_{co1} and v_{co2} and their magnified views

VII. Experimental Verification

A 1.5 kW laboratory prototype of the proposed inverter is fabricated and detailed experimental studies have been carried out to demonstrate the effectiveness of the proposed scheme. The parameters as mentioned in Table I are used to realize the laboratory prototype of the inverter. In order to realize PV_1 and PV_2 two programmable EPS PSI9360-15 power supplies having solar PV emulation feature are utilized. The photograph of the experimental prototype is shown in Fig. 10.

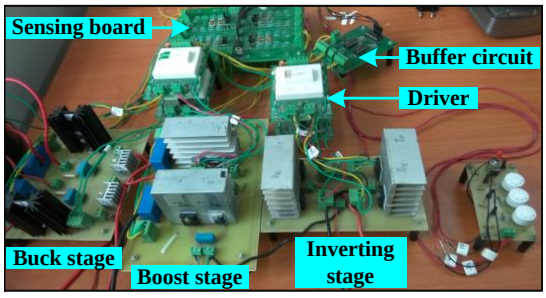

Fig. 10. Experimental prototype of the proposed inverter

The EPS PSI9306-15 power supply has the provision to change only the effect of insolation level while the option to change the effect of temperature is unavailable. In order to emulate simultaneous variation in temperature and level of insolation, the MPP parameters of the two solar emulators (solar emulator 1 as PV_1 and solar emulator 2 as PV_2) are set as follows at STC: V_{pv1} = 130 V, I_{pv1} = 5 A and V_{pv2} = 120 V, I_{pv2} = 5 A. The variation in insolation level of PV_1 is indicated in Table III while the insolation level of PV_2 is maintained at 80%. The expected values of I_{pv1}, I_{pv2}, P_{pv1}, P_{pv2}, V_{co1m}, V_{co2m}, I_{gm}, I_{L1m}, I_{L2m} for the entire operating range are tabulated in the Table III. Fig. 11 depicts the change in i_g, I_{pv1}, I_{pv2}, P_{pv1}, P_{pv2} throughout the range of variation in the level of insolation as specified in Table III. Magnified version of the responses of v_{co1}, v_{co2}, i_{L1} and i_{L2} along with v_g, i_g are also shown in Fig. 12(a) to (f) for two different insolation levels of PV_1. The figures Fig. 12(a) and (b) ensure that i_g remains to be sinusoidal and in-phase with v_g in spite of having difference in the magnitude of power being extracted from the two subarrays. From Fig. 12(c) it can be inferred that the converter associated with PV_1 operates completely in buck mode, whereas the converter associated with PV_2 operates in both buck and boost mode depending on the requirement. Thus it can be inferred that the two converter segments are able to operate in a decoupled fashion. The measured variables, I_{pv1}, I_{pv2}, P_{pv1}, P_{pv2}, V_{co1m}, V_{co2m}, I_{gm}, I_{L1m}, I_{L2m} as depicted in Figs. 11, 12 are more or less same as that of the estimated ones presented in Table III, and this validates the ability of the proposed inverter to extract maximum power from two subarrays operating under MEC.

TABLE III
Estimated variation in I_{pv1}, I_{pv2}, P_{pv1}, P_{pv2}, V_{co1m}, V_{co2m}, I_{gm}, I_{L1m}, I_{L2m} during PV_1 insolation variation

% Insol. of PV_1	40	50	60	70	80	90	100
% Insol. of PV_2	80	80	80	80	80	80	80
I_{pv1} (A)	2	2.5	3	3.5	4	4.5	5
I_{pv2} (A)	4	4	4	4	4	4	4
P_{pv1} (W)	260	325	390	455	520	585	650
P_{pv2} (W)	480	480	480	480	480	480	480
V_{co1m} (V)	109	126	140	151	162	171	179
V_{co2m} (V)	202	185	171	160	149	140	132
I_{gm} (A)	4.6	5	5.4	5.8	6.2	6.6	7
I_{L1m} (A)	4.6	5	5.8	6.8	7.8	8.7	10
I_{L2m} (A)	7.7	7.7	7.7	7.7	7.7	7.7	7.7

Fig.13 depicts the Fast Fourier Transform (FFT) of i_g. The THD of i_g is found to be 4.61% which is below the limit of 5% as specified in the standards, IEEE 1574/IEC 61727 [22]. It may be noted that the measured THD of v_g is found to be 2.12% and hence the contribution to THD from the inverter is much less than 4.61%.

The measured and estimated efficiency curves of the proposed inverter are shown Fig.14. In order to measure the efficiency of the proposed inverter the Yokogawa make power analyzer, WT1800 is used and further, the losses incurred in the active and passive elements of the power circuit is considered while the losses involved with the control circuit are neglected. The efficiency is determined while both V_{pv1} and V_{pv2} are set at 130 V. Measured peak efficiency is found to be 97.65% and the measured European efficiency (η_{euro}) is obtained as 97.02%.

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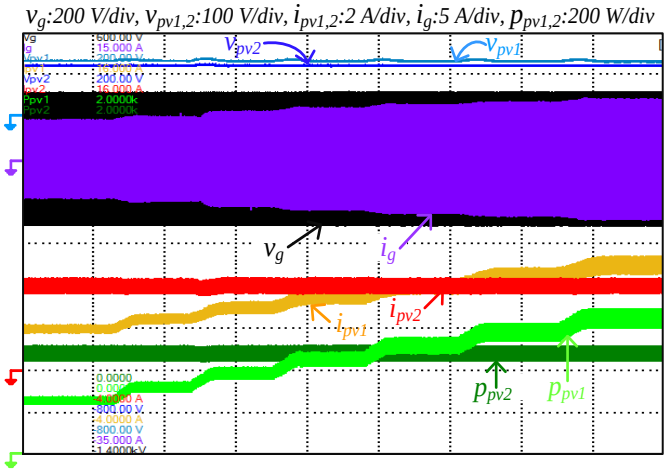

Fig. 11. Experimental waveforms: v_{pv1}, v_{pv2}, i_g, v_g, i_{pv1}, i_{pv2}, p_{pv1}, p_{pv2} throughout the entire operating range

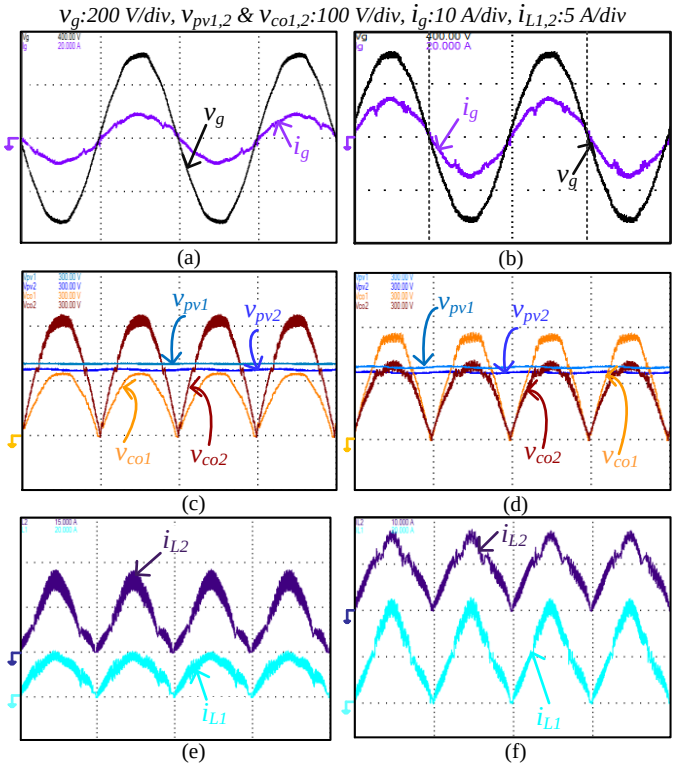

Fig. 12. Experimental waveforms: Magnified version of i_g, v_g when (a) insolation of PV_1=40% & insolation of PV_2=80%, (b) insolation of PV_1=100% & insolation of PV_2=80%, magnified version of v_{pv1}, v_{pv2}, v_{co1}, v_{co2} when (c) insolation of PV_1=40% & insolation of PV_2=80%, (d) insolation of PV_1=100% & insolation of PV_2=80%, magnified version of i_{L1}, i_{L2} when (e) insolation of PV_1=40% & insolation of PV_2=80%, (f) insolation of PV_1=100% & insolation of PV_2=80%

In order to measure the leakage current involved with the proposed inverter, 0.1 μF polypropylene film capacitors are used to emulate C_{pv1} and C_{pv2}. Fig. 15 depicts the voltages that appear across C_{pv1} and C_{pv2}, and the leakage currents, i_{cpv1} and i_{cpv2} flowing through C_{pv1} and C_{pv2}. The measured waveforms of v_{cpv1} and v_{cpv2} show that they contain signif-

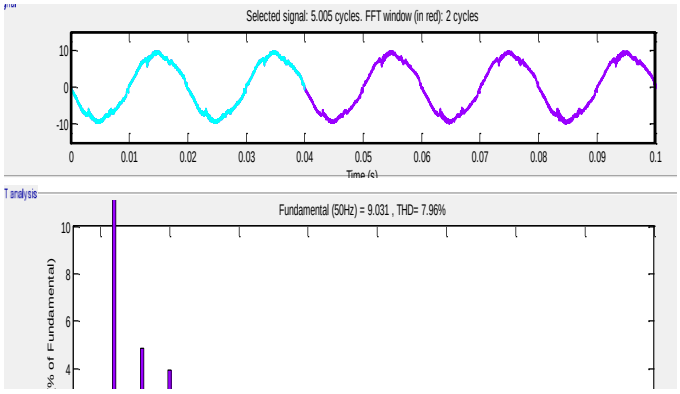

Fig. 13. Experimental waveform: FFT of i_g

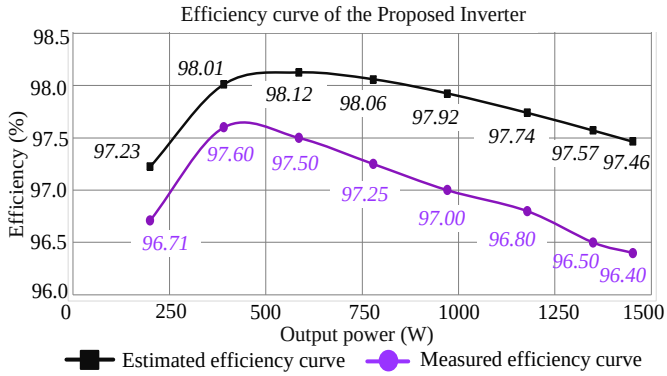

Fig. 14. Efficiency curves of the Proposed inverter

icant amount of dc and low frequency components whereas presence of high frequency components are negligible. The measured RMS value of total leakage current is found to be 80.7 mA which is much lower than the limit 300 mA as specified in the standard, VDE 0126-1-1, and also cited in [23].

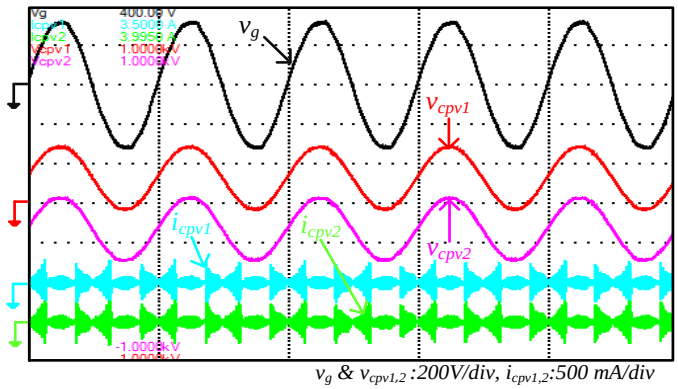

Fig. 15. Experimental waveform: v_g, v_{cpv1}, v_{cpv2}, i_{cpv1}, i_{cpv2}

In order to demonstrate the stability of the proposed scheme in the event of a disturbance in v_g, a step change of 70 V (150 V to 220 V) is introduced in v_g while V_{pv1} and V_{pv2} are kept at 130 V and the references for the current controllers are

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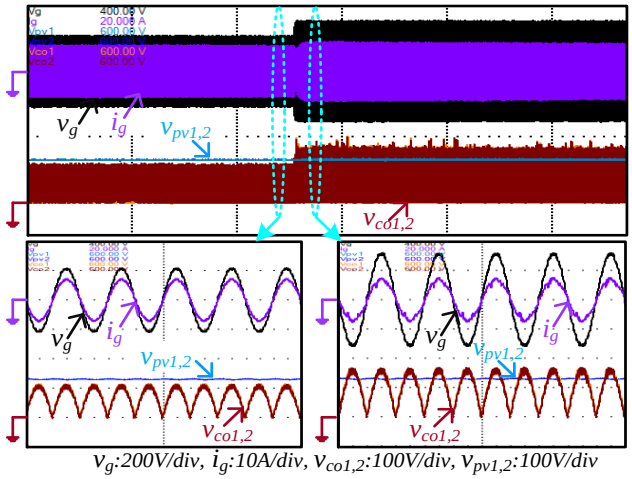

Fig. 16. Experimental waveform: v_g, i_g, v_{co1}, v_{co2}, v_{pv1}, v_{pv2} when v_g is changed from 150 V to 220 V

purposely set at a fixed value in each mode. The response of the system during the aforesaid test condition where mode of operation of the proposed inverter is shifted from buck mode to buck and boost mode is shown in Fig. 16. It can be inferred from the Fig. 16 that the system can effectively ride through situations arising due to the disturbances in v_g.

A comparison of various features of the proposed scheme with existing transformerless schemes such as NPC based scheme [5], H-Bridge based scheme [2], schemes presented in [18] and [21] has been performed and presented in Table IV. Following issues are considered for carrying out this comparison: i) solar modules, Canadian solar 'CS6P-165PE' [25] are utilized for the purpose, ii) Minimum input voltage requirement for NPC based scheme [5] and H-Bridge based scheme [2] is taken to be 800 V and 400 V respectively while minimum input voltage requirement of the schemes presented in [18], [21] and that of the proposed scheme is taken to be 230 V, iii) for simplicity total area required for a system is determined by multiplying the total number of modules required with the area of a single module. The nomenclatures used in the Table IV are defined as follows: N_{PVR} = required number of PV arrays/subarrays, N_{PVC} = number of PV arrays controlled simultaneously, V_{IN} = input voltage requirement, N_{MS} = number of modules connected in series in a PV string of a PV array/subarray which is made with a single string, N_{MT} = minimum number of modules required to design the PV system, P_{SYS} = minimum power rating of the PV system, A_{PV} = minimum area required to install all PV modules, E_{MEC} = possibility to get affected by MEC which is determined from Table V. Based on the objective comparison presented in the Table IV it can be inferred that the proposed inverter deals with MEC in the most effective way.

In order to compare the power extraction from PV array by various transformerless schemes as mentioned in Table IV while the schemes are operating under MEC, a 5.3 kW PV system at STC, built with 32 'CS6P-165PE' Canadian solar modules [25] is considered. Depending on the minimum DC voltage requirement, type of input connection required

TABLE IV
COMPARISON TABLE OF VARIOUS TRANSFORMERLESS SCHEMES

Schemes	N_{PVR} & N_{PVC}	V_{IN} (V)	N_{MS} & N_{MT}	P_{SYS} (kW)	A_{PV} (m^2)	E_{MEC}
NPC based [5]	1 & 1	$> 2V_m$	28 & 28	4.6	44.8	Highest
H-Bridge based [2]	1 & 1	$> V_m$	14 & 14	2.3	22.4	High
Reported in [18]	2 & 2	$< V_m$	8 & 16	2.6	25.6	Low
Reported in [21]	1 & 1	$< V_m$	8 & 8	1.3	12.8	Low
Proposed DBBI	2 & 2	$< V_m$	4 & 8	1.3	12.8	Lowest

TABLE V
EFFECT OF MEC IN DIFFERENT TRANSFORMERLESS SCHEMES

	Mod_{1in} (%)	100	90	80	70	60	50
Schemes	P_{avl} (kW)	5.3	5.27	5.25	5.24	5.22	5.2
NPC based [5]	P_{ext} (kW)	5.3	5.2	4.9	4.53	4.1	3.6
	P_{diff} (kW)	0	0.07	0.35	0.71	1.12	1.6
	P_{lost} (%)	0	1.3	6.7	13.5	21.7	31.5
H-Bridge based [2]	P_{ext} (kW)	5.3	5.23	5.04	4.8	4.54	4.25
	P_{diff} (kW)	0	0.04	0.21	0.44	0.68	0.95
	P_{lost} (%)	0	0.8	4	8.2	13.1	18.3
Reported in [18]	P_{ext} (kW)	5.3	5.25	5.15	5.03	4.90	4.75
	P_{diff} (kW)	0	0.02	0.1	0.21	0.32	0.45
	P_{lost} (%)	0	0.4	2	4	6.1	8.6
Reported in [21]	P_{ext} (kW)	5.3	5.25	5.15	5.03	4.90	4.75
	P_{diff} (kW)	0	0.02	0.1	0.21	0.32	0.45
	P_{lost} (%)	0	0.4	2	4	6.1	8.6
Proposed DBBI	P_{ext} (kW)	5.3	5.26	5.21	5.14	5.08	5.01
	P_{diff} (kW)	0	0.01	0.04	0.1	0.14	0.19
	P_{lost} (%)	0	0.2	0.8	2	2.7	3.6

and power rating of the schemes, required number of PV modules are connected in series-parallel combination to form PV array/subarrays. The PV arrays/subarrays of the schemes are configured as follows: i) N_{MS} = 32 in [5], ii) N_{MS} = 16 and N_{MP} = 2 in [2], wherein N_{MP} = number of strings connected in parallel in an array/subarray, iii) N_{MS} = 8 and N_{MP} = 2 in [18], iv) N_{MS} = 8 and N_{MP} = 4 in [21], v) N_{MS} = 4 and N_{MP} = 4 in DBBI. Further, it is also assumed that no parallel diode is connected across PV modules. The insolation level of one module, Mod_{1in} is varied from 100% to 50% with a step of 10% while the insolation of rest of the 31 modules are kept at 100%, i.e. at STC. The total estimated extracted power from the PV subarrays during MEC by any scheme, P_{ext} = power of affected string + power of rest of the string, the actual available maximum power in the PV array of any scheme, P_{avl} = 31xpower of each module + power of affected module, their difference, P_{diff} and the percentage loss of power due to MEC in any scheme, P_{lost} are tabulated in Table V. As the effect of MEC is less severe in parallel connected PV strings, the aforementioned effect is neglected to avoid complexity in calculation. From Table V it can be concluded that the proposed inverter is the most effective solution in extracting power during MEC.

VIII. CONCLUSION

A single phase grid connected transformerless buck and boost based PV inverter which can operate two subarrays at their respective MPP was proposed in this paper. The attractive features of this inverter were i) effect of mismatched environmental conditions on the PV array could be dealt with

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in an effective way, ii) operating efficiency achieved, η_{euro} = 97.02% was high, iii) decoupled control of component converters was possible, iv) simple MPPT algorithm was employed to ensure MPP operation for the component converters, v) leakage current associated with the PV arrays was within the limit mentioned in VDE 0126-1-1. Mathematical analysis of the proposed inverter leading to the development of its small signal model was carried out. The criterion to select the values of the output filter components was presented. The scheme was validated by carrying out detailed simulation studies and subsequently the viability of the scheme was ascertained by carrying out thorough experimental studies on a 1.5 kW prototype of the inverter fabricated for the purpose.

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